List of Claims:

Claim 1 (original): A semiconductor manufacturing process for forming the active region of a Silicon-On- Insulator (SOl) device comprising the steps of:

providing a bulk substrate having a buried oxide layer thereon and having a thin undoped SOl silicon layer atop said buried oxide layer;

depositing a polysilicon layer atop said SOl silicon layer and patterning a gate feature out of said polysilicon layer, said SOl silicon layer having a top surface, said gate feature having sidewalls and a top and bottom surface, said top surface of said gate feature being further distant from said SOl silicon layer than said bottom surface of said gate feature;

forming dielectric sidewall spacers abutting said gate feature sidewalls;

etching through said top surface of said gate feature to form a first and a second tapered polysilicon feature, each said first and second tapered polysilicon feature having a base and a top, said bases being wider than said tops, each said tapered polysilicon feature having a tapered surface connecting said base to said top opposite said abutting dielectric sidewall spacers, said first and second tapered polysilicon features having a gap therebetween, said gap having a bottom edge, said bottom edge of said gap being a portion of said top surface of said SOl silicon layer and said bottom edge of said gap having a length;

depositing a gate dielectric onto said bottom edge of said gap and onto said tapered surfaces of said tapered polysilicon features; and

depositing metal onto said gate dielectric to fill said gap.

Claim 2 (original): The semiconductor manufacturing method of claim I, wherein said length of said bottom edge of said gap is less than 50 nm.

Claim 3 (original): The semiconductor manufacturing method of claim 2, further including the steps of:

before said step of depositing said polysilicon layer, forming a temporary gate dielectric layer atop said SOI silicon layer;

after depositing said polysilicon layer and prior to patterning said gate feature, depositing a layer of SiON atop said polysilicon layer, said patterned gate feature thereby having a layer of SiON atop said polysilicon, said SiON layer having a top surface;

after said step of patterning said gate feature and prior to said step of forming said dielectric sidewall spacers, implanting extension regions in said SOl silicon layer and annealing said implanted extension regions;

said step of forming dielectric sidewall spacers removing a portion of said temporary gate dielectric not below said gate feature;

after said step of forming dielectric sidewall spacers, implanting source/drain regions in said SOl silicon layer and annealing said implanted source/drain regions;

after said step of implanting said source/drain regions, forming a silicide layer on exposed regions of said SOl silicon layer;

after said step of forming a silicide layer, depositing a layer of TEOS and polishing said TEOS layer to said top surface of said SiON layer; and wherein

said step of depositing said gate dielectric and said step of depositing said metal onto said gate dielectric are performed at temperatures below 800 C.

Claim 4 (original): The semiconductor manufacturing process of claim 2, wherein:

said step of etching through said gate feature to form said tapered polysilicon features is performed by Reactive Ion Etching utilizing a mixture of HBr and $C1_2$ etch gases;

said step of depositing said gate dielectric comprises Remote Plasma Processing;

said step of depositing said metal onto said gate dielectric is performed using a method selected from the group consisting of: CVD, PVD, electroplating, and Atomic Layer Deposition.

Claims 5- 6 (cancelled)

Claim 7 (original): An FDSOI device having an active region, said active region being formed by the process of claim 2.

Claim 8 (cancelled)

Claim 9 (original): An FDSOI device comprising:

a bulk semiconductor substrate having a top surface, a buried oxide layer atop said top surface of said substrate and a thin undoped SOl silicon layer atop said buried oxide layer thereon, said buried oxide layer having a thickness in the range between 50 and 60 nm, and said SOl silicon layer having a top surface and having a thickness in the range between 5 and 20 nm;

a doped gate poly feature on said top surface of said SOl silicon layer, said doped gate poly feature having a length in the range between 40 and 75 nm, said doped gate poly feature having outer sidewalls, said doped gate tapered polysilicon features each having a base and a top, each said base being wider than said top, each said tapered polysilicon feature having a tapered surface connecting said poly feature comprising a first and a second tapered polysilicon feature having a gap therebetween, said first and second base to said top opposite said outer sidewalls, said tapered surfaces being at an angle with respect to said top surface of said bulk substrate, said gap having a bottom edge, said bottom edge of said gap being a portion of said top surface of said SOl silicon layer and said bottom edge of said gap having a length;

said doped gate poly feature has a pair of extension implanted regions in said SOl silicon layer, said extension implanted regions extending under said first and second tapered polysilicon features;

said doped gate poly feature has a pair of dielectric spacers abutting said gate poly feature outer sidewalls, said dielectric spacers having a top and a bottom; and

source/drain implanted regions in said SOl silicon layer, said source/drain implanted regions extending under said dielectric spacers.

Claim 10 (original): The device of claim 9 further comprising:

a layer of cobalt silicide atop a portion of said SOl silicon layer not under said gate poly feature or said dielectric spacers; and

a TEOS layer atop said cobalt silicide layer, said TEOS layer having a thickness in the range between 150 and 200 nm, said TEOS layer having a top surface, said top surface of said TEOS layer being substantially even with said top of said dielectric spacers.

Claim 11 (cancelled)

Claim 12 (new): A method of manufacturing a Silicon-On-Insulator (SOI) structure, said method comprising the steps of:

fabricating a MOS structure including a ploysilicon gate;

forming dielectric spacers abutting sidewalls of said ploysilicon gate;

taper-etching said ploysilicon gate to form tapered poly spacers separated by a gap;

depositing a gate dielectric into said gap; and

depositing a metal on said gate dielectric and into said gap.

Claim 13 (new): The method of claim 12, wherein said step of depositing said metal forms a metal gate, and wherein said metal gate is less than 50 nm in length.

Claim 14 (new): The method of claim 12, wherein said step of taper-etching uses Reactive Ion Etching utilizing a mixture of HBr and Cl_2 etch gases.

Claim 15 (new): The method of claim 12, wherein said step of taper-etching includes:

adjusting a temperature to be in a range of 30° C to 70° C;

adjusting Cl_2/HBr gas flow ratio to be in a range of 0.5 to 1.5; and

adjusting a taper angle to be in a range of 75° to 85°.

Claim 16 (new): The method of claim 15, wherein said step of depositing said metal forms a metal gate, and wherein said metal gate is less than 50 nm in length.

Claim 17 (new): A Silicon-On-Insulator (SOI) structure comprising:

a MOS structure including a ploysilicon gate;

dielectric spacers abutting sidewalls of said ploysilicon gate;

tapered poly spacers separated by a gap, wherein said tapered poly spacers are formed by taper-etching said ploysilicon gate;

a gate dielectric in said gap; and

a metal on said gate dielectric and in said gap.

Claim 18 (new): The SOI structure of claim 17, wherein said metal forms a metal gate, and wherein said metal gate is less than 50 nm in length.

Claim 19 (new): The SOI structure of claim 17, wherein said taper-etching uses Reactive Ion Etching utilizing a mixture of HBr and Cl_2 etch gases.

Claim 20 (new): The SOI structure of claim 17, said taper-etching is achieved by adjusting a temperature to be in a range of 30° C to 70° C, adjusting Cl_2/HBr gas flow ratio to be in a range of 0.5 to 1.5, and adjusting a taper angle to be in a range of 75° to 85°.

Claim 21 (new): The SOI structure of claim 20, wherein said metal forms a metal gate, and wherein said metal gate is less than 50 nm in length.